	Type	Hits	Search Text	DBs	Time Stamp
247	BRS	94	current same density and (transient same analysis) and (integrated adj circuit)	USPAT; US-PGPUB; DERWENT	2003/01/29 15:37
248	BRS	30	current same density and (transient same analysis) and (integrated adj circuit) and verification	USPAT; US-PGPUB; DERWENT	2003/01/29 14:30
249	BRS	733	spice same (simulation or analysis) and (integrated adj circuit)	USPAT; US-PGPUB; DERWENT	2003/01/29 15:37
250	BRS	49	(spice same (simulation or analysis) and (integrated adj circuit)) and current adj density	USPAT; US-PGPUB; DERWENT	2003/01/31 10:12

	Type	Hits	Search Text	DBs	Time Stamp
243	BRS	527	transient same analysis and (integrated adj circuit)	USPAT; US-PGPUB	2003/01/28 10:24
244	BRS	118	transient same analysis and (integrated adj circuit) and verification	USPAT; US-PGPUB; DERWENT	2003/01/28 10:25
245	BRS	146	transient same analysis and ((integrated adj circuit) or semiconductor) and verification	USPAT; US-PGPUB; DERWENT	2003/01/28 11:23

	Type	Hits	Search Text	DBs	Time Stamp
197	BRS	6	circuit same verification same simulation same (operating near conditions)	USPAT; US-PGPUB; EPO; DERWENT	2003/01/14 10:25
198	BRS	64	circuit same simulation same verification same (voltage or current)	USPAT; US-PGPUB; EPO; DERWENT	2003/01/14 10:27
199	BRS	36	circuit same simulation same verification same (voltage or current) and specification	USPAT; US-PGPUB; EPO; DERWENT	2003/01/14 12:11

Automatic functional model validation between SPICE and Verilog

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This paper appears in: **Industry Applications Conference, 1995. Thirtieth IAS Annual Meeting, IAS '95., Conference Record of the 1995 IEEE**
10/08/1995 -10/12/1995, 8-12 Oct 1995
Location: Orlando, FL , USA
On page(s): 1076-1083 vol.2
8-12 Oct 1995
INSPEC Accession Number: 5144894

Abstract:
This paper outlines the development of a validation methodology suitable for testing and qualification of ASIC libraries. In particular this paper outlines a method which uses SPICE models in conjunction with Verilog models to validate the functionality of a Verilog library

Index Terms:
ASIC model libraries SPICE Verilog application specific integrated circuits automatic functional model validation circuit analysis computing computer simulation integrated circuit modelling integrated circuit testing qualification testing

Sp2V: accelerating post-layout spice simulation using Verilog gate-level modeling

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This paper appears in: **Electrical and Computer Engineering, 2001. Canadian Conference on**
05/13/2001 -05/16/2001, 2001
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2001
Number of Pages: 2 vol.1414
INSPEC Accession Number: 7068713

Abstract:
We propose a system for accelerating post-layout simulation of digital circuits. The conventional method using standard cells for layout generation leads us to perform post-layout simulation of digital circuits at the gate-level rather than the transistor or switch level. In our method, first an accurate model of each standard cell or gate is described in Verilog HDL. Then the Verilog model of design, which uses instances of gates, is generated from the corresponding Spice description through an automatic method. The result of the proposed method has a simulation gain of one to two orders of magnitude with exact functionality and a maximum 15% timing accuracy less than Spice simulation, as well as providing a complete design into high-level description, which alleviates many SPICE problems like convergence and other failures especially in large designs

Index Terms:
cellular arrays circuit layout CAD circuit simulation delays digital circuits hardware

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Page(s): 464 -469

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